Testing using the JTAG Interface

Checking interconnections without test pins. Testing printed circuit boards by hand is difficult, if not impossible, when using complex ICs and multilayer printed circuit boards. Fortunately most of these ICs now contain special logic which allows extensive testing of the chip’s internal connections and the interconnections on the circuit board. This is achieved by using the internationally standardised JTAG-interface.

Demanding Test Requirements for High density FPGA and Processor Based Boards

As we know chip density and packaging have become both higher and physically smaller in size as the Electronics industry demands smaller products with more functionality. The result is chip packaging and interconnectivity have become more dense and operate at higher clock frequencies. Physical access for traditional bed-of-nails testing becomes limited some times even impossible. This causes loss of ICT (in-circuit test), fault coverage and higher test fixture costs. Reduced fault coverage, coupled with limited diagnostic resolution at CIT and FT (functional test), often add up to excessive debug times which can cause costly delays, extended repair cycles and perhaps work only partially. So how do we find the problem, is it the design or is it because a few parts aren’t mounted correctly or do we have interconnect problems in the form of opens or shorts.

Quickly you will reach for an oscilloscope or multimeter to verify whether the signals are correct or to check the connections between parts. These days, with multilayer boards containing fine-pitch and/or BGA components this is practically impossible. So how can you test these boards?

A frequently used method is a functional test

Using special software test-routines the functionality of the board is examined. An important prerequisite of this is that the core of the circuit is functional; if it is not, then you cannot proceed with a functional test. Diagnosing the actual fault using a functional test can be very difficult. For example, the functional test may indicate that there is a problem with the memory but however will not show you to the pin(s) that is causing the problem.

You can also choose to do a structural test.

If all the components on the printed circuit board are correctly soldered – the board should work – assuming the design is correct and the components are OK. In other words: the objective is to prove that all components are soldered correctly. The simplest method is to use a multimeter to carry out a continuity test between all components. (See Fig. 1).

The main advantage of a structural test is that it will pinpoint to the exact location of the problem. A pin that’s not soldered properly or is shorted to another pin is immediately discovered. In order to obtain optimal test coverage and to be able to get the best diagnostics it is necessary to have a large number of testpoints. For this purpose test pads are often added to the board. However, test pads cost money, require extra space and may act as antennas picking up noise.

So modern designs with high component density have an immediate problem, on
In the late 80s and early 90s, in-circuit emulation (ICE) was a popular approach for processor based boards. However, its decline was driven by the absence of socketed processors and ROM devices in new designs. This resulted in the establishment of the JTAG (Joint Test Action Group) and the resulting IEEE 1149.1 standard. Today almost all processors, FPGA and large scale peripherals devices have an incorporated JTAG port.

Whilst primarily born out of the need to overcome test access problems of fine-pitch components including BGAs, the JTAG port now offers the ability to access internal registers and memories, as well as the ability to apply breakpoints, similar to the emulators of the past, but without being obtrusive, slowing the processor, or requiring target system hardware or software resources. JTAG provides all of the capabilities of a debugger while offering the potential for functional testing of a unit-under-test (UUT) at full operating speed. JTAG also opens up the possibility of marrying boundary-scan based structural testing with functional testing as a straightforward alternative or extension to a test strategy based solely on ICT.

Simply stated, boards with bus architecture allow on-board emulation to take over control via one of the buses. This allows emulation to take full control over all of the processor buses. The result is a debug interface port which offers synergic benefits up-stream (board design) and down-stream (board test). These benefits enable users to exploit JTAG to enhance structural and functional test coverage potential for boundary-scan as well as non-boundary-scan devices. So, how is the potential realised? By employing a unique hybrid approach, combining the benefits of boundary-scan and JTAG functional testing environment.

The Boundary Scan (Bscan) architecture

Take a microcontroller as an example. In addition to the core, which provides the actual functionality of the chip, the silicon also accommodates the necessary hardware for Bscan. This additional hardware consists of, among others, a Bypass – an Instruction – a Boundary Scan register and a controller. The Bscan register (BSR) is formed from transparent cells sitting between the I/O pins and the core. There are also four or five additional pins: TDI (test data in), TDO (test data out), TCK (test clock), TMS (test
How does Boundary Scan work?

By inserting the BSR into the TDI→TDO path, any arbitrary bit pattern can be shifted into the Bscan cells via the TDI pin. By issuing an "Update" instruction the data in the BSR is put onto the I/O pins.

In the opposite manner, the "Capture" instruction reads the data at the I/O pins and copies it into the BSR. The contents of the BSR can then be shifted out via TDO. These two actions of "driving" and "sensing" are used to test the connections between components.

Example 1

By connecting the TDO of a Bscan chip to the TDI of a next one, a Bscan chain is formed. To ensure correct synchronisation the TCK and TMS signals of the TAP are directly connected to each chip individually (see Fig. 4). In principle, an unlimited number of Bscan components can be cascaded to form the chain. However, for practical reasons this is usually limited to about 10 Bscan components.

In the above example a chain of two Bscan components is used, a microcontroller and an FPGA. The total chain comprises the Bscan cells of IC1 plus the Bscan cells of IC2. According to the schematic, the I/O pins of IC1 and IC2 are connected to each other via interconnects Net_1 through Net_5. The question is to verify whether this is actually the case on the circuit board. In other words: we have to check if there are no opens or shorts between the nets.

The first step is to shift in a test vector "11111" into the BSR so that the Bscan cells of IC1 that belong to Net_1–Net_5 contain logic ones. (See Fig. 5).

Note that during shifting data in/out of the BSR the actual state of the I/O pins does not change. Only after sending the "Update" command, data from the BSR is put onto the
I/O pins. In this case the vector “11111” is now on Net_1–Net_5 (see Fig. 5).

The next step is to read the data which is on Net_1–Net_5 into the corresponding Bscan cells of IC2 using a “Capture” command. (See Fig. 6).

Now the entire content of the BSR is shifted out. Software is then used to compare the vector obtained with the vector that was expected. The latter has to be ‘11111’, however the vector read back is ‘11011’. The bit that was read for Net_3 is a ‘0’, while a ‘1’ was expected. This indicates that there is a problem with Net_3. By using a number of clever test vectors it is possible to diagnose that there is an open circuit under the I/O pin of IC2. In this manner it is possible to quickly pinpoint opens, shorts between individual nets and shorts to Vcc or Gnd.

In this example we assumed only five connections, in practice there will easily be several tens to hundreds of connections that can be tested in this way.

The above explained how the connections between Bscan components can be tested. In this framework it is important to note that this method works with components that comply with the IEEE119.1 Boundary-scan standard (Bscan compliant).

However the average board, in addition to one or more Bscan compliant chips also contains a large number of non-Bscan compliant devices such as resistors, RAM, flash memory, I/O, connectors, etc. It is possible to use Bscan for these as well (see Example 2).

Example 2

Fig. 7 is a circuit board which contains a μC, FPGA, RAM, flash memory and I/O. Only the μC and FPGA are Bscan compliant. For clarity, the Bscan chain is symbolically indicated with a thick green line through these components.

The Bscan chain has direct access to the I/O pins of the μC and the FPGA and therefore also to the bus, which contains the address-, data- and control lines. Using the JTAG interface, there is therefore direct access to the connecting pins of the RAM, Flash and I/O.

To test whether the RAM is connected correctly, special test patterns are shifted into the BSR via the JTAG interface. These test patterns consist of address-, data- and control bits. By choosing appropriate data patterns, Bscan can write/read into the RAM. Based on these results it is possible to determine whether all the pins of the memory chip are connected properly and in the case of a fault, it will pinpoint to the pin that is causing the problem.

In a similar manner, it is also possible to test the connectivity of the flash.

For the testing of the I/O block including the connectors this example uses an external Bscan module with an adequate number of I/O pins. These pins are connected to the connectors on the board. The BSR of the I/O module is connected in series with the chain on the board (Fig. 8). In this way the Bscan has complete access to the connectors and the I/O block on the circuit board and these can be included in the test.

Programming

After all the board interconnects have been tested for any potential defects, the JTAG interface is used to program the Flash and optionally μC, and to configure the FPGA.

“Real world examples”

One of the EDA design system of choice is Altium as they provide automatic test point test information and netlist information that conforms to the IEEE 1149.1 standard. So if you have designed your product using Altium you could have test points automatically inserted into your design using their test point wizard. Using these test points, component information and netlist information a board coverage profile can be established using the tools supplied by JTAG Technologies. Using Altium one can insert test points or probes in the schematic these traces can then be stimulated or viewed all the way from schematic design via the circuit board layout to the assembled PCB. Another approach would be to use a combination of Altium and tools supplied by JTAG Technologies. Software such as JTAG ProVision, the professional/visual development system from JTAG Technologies this delivers the ultimate in ease of use while meeting your need for a high-performance, high-quality development tool. Because it requires minimal boundary-scan knowledge and little design detail, ProVision enables you to generate applications quickly, focusing on optimising the testability of your designs. Boundary-scan topology is analysed automatically, even for complex multi-chain arrangements. Models for thousands of different non-boundary-scan devices allow JTAG ProVision to automatically control signals on your board for optimum test coverage and ISP performance while providing safe conditions on all board components.

In conclusion

Boundary scan is eminently suitable for testing and on-board programming of digital circuit boards. Bscan can also be used in conjunction with non-Bscan components. Since many designs already use Bscan-compliant devices, such as μCs and FPGAs, the number of test pads can be greatly reduced. As a consequence, expensive test fixtures become unnecessary or can be greatly simplified. Thanks to good diagnostics a problem can be located quickly; functional test times can be slashed from minutes to seconds. Additionally, boundary-scan structural tests can be executed in advance of functional tests, providing more detailed resolution during fault detection therefore many designers and manufacturing companies recognise these advantages and already use Boundary-scan successfully.


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