New algorithm for generator differential protection

by B Kasztenny and D Finney, General Electric Multilin, Canada

External fault currents combined with long DC time constants expose current transformers (CTs) of generator protection to substantial saturation. Still, in many cases generator protection CTs are not selected and/or matched properly.

This is particularly true in industrial applications, where small machines, co-generators or distributed generators, use underrated CTs. This is often driven by economic, not technical considerations and calls for better performance of protective relays. In other cases, the trend towards more compact switchgear does not allow for CTs with a generous rating.

Cases are reported where significant saturation of main CTs could occur under relatively small currents (as low as twice the nominal) in as little as a few power system cycles. Quite often, different engineering teams select the neutral-side CTs and terminal-side CTs: not only are the CT characteristics and burden impedances not matched, but also the CTs may come from two different manufacturers. As a result, distant external faults, transformer inrush currents, or sudden changes in the load could result in CT saturation and misoperation of stator differential protection if set too sensitive.

Traditional means of dealing with CT saturation would fall under such conditions. The currents are small thus no significant restraint is produced. The relay would typically apply the lower slope of its characteristic and would misoperate even if only a small spurious differential current is produced by the saturated CT. CT saturation mechanisms often built into the differential protection of more advanced relays would also fail because they are typically designed to cope with AC saturation under large through currents. This paper presents research and implementation of enhanced stator differential protection driven by industrial applications where the CTs were selected first, and the relays were selected later with the primary criterion to handle the grossly underrated or mismatched CTs.

First, a novel CT saturation detection algorithm is implemented. The detection algorithm incorporates two distinctive parts. One is aimed at identifying AC saturation under large currents, while the other is aimed at detecting DC saturation under small currents such as transformer inrush or a sudden change of load.

Second, a phase comparison principle is incorporated to make the protection secure. The phase comparison algorithm applies adaptive thresholds in order to ensure good sensitivity.

Third, the three major elements: differential, saturation detection, and directional units are combined using adaptive logic in order to provide for fast, sensitive and secure protection.

Sample results of testing of a commercially available relay incorporating the new algorithm are included.

**Differential characteristic**

The input currents are sampled at 64 samples per cycle and pre-filtered using an optimized MMIC filter aimed at removing DC component(s) and other low-frequency oscillations. The optimized filter is a Finite Response Filter (FIR) with the window length of approximately 1/3rd of power system cycle. The digitally pre-filtered currents are converted into phasors by applying the full-cycle Fourier filter. The full-cycle window combined with the optimized MMIC filter allows for excellent filtering (Fig. 1). At the same time owing to the differential operating principle and unique definition of the restraining signal, the differential algorithm responds to internal faults in less than half-a-cycle, which meets our design criteria.

The operating current is produced as per the principle of differential protection (the entire algorithm is phase-segregated – the phase index is omitted in this paper):  
$$ ID = |I_D| - |I_T| $$  

where subscripts D, T and N stand for differential, terminal-side and neutral-side currents, respectively and $| |$ stands for phasor magnitude.

The restraining current is produced as the greater of the two currents:

$$ I_{R1} = \max (|I_D|, |I_T|, |I_N|) $$ (2)

The “maximum of” definition of the restraining current brings in two advantages. First, during heavy internal faults, the ratio between the differential and restraining currents is much higher than 100%, resulting in fast and reliable operation. Second, during an external fault with saturation of one set of CTs, the restraining current is not reduced by the saturation as long as one of the CTs (neutral or terminal) is not saturated. Differential relays must cope with switch-off transients. An external fault may saturate one or more CTs and bring the differential-restraining point close to the operating line of the characteristic. When the
external fault is subsequently cleared, both
the differential and restraining currents start
decreasing. The resulting switch-off trajectory
may temporarily enter the characteristic and
cause misoperation (Fig. 2a). A crude way of
preventing this from happening is to delay
intentionally – after detecting a fault but not
operating for it – operation of the differential
function.

As delaying – even conditionally – operation
of protection is not desired, the algorithm
presented in this paper applies instead
additional post-filtering to the raw restraining
current in order to cope with switch-off
transients. The effective restraining current is
a maximum instantaneous value in the last
power system cycle:

\[ I_{R(k)} = \max (I_{R1(k-p)}) \quad p = 0..1 \text{ cycle} \quad (3) \]

When clearing an external fault that has
just heavily saturated the CTs and thus has
produced a spurious differential current, it
will take approximately one full cycle for such
spurious differential current to disappear.
During that time the restraining current (3)
– owing to its one-cycle memory – does not
decrease at all. This results in a well-behaved
switch-off trajectory (Fig. 2a).

The presented algorithm uses a dual-slope
dual-break-point operating characteristic
when comparing the operating signal (1)
with the effective restraining signal(3). Both
the slope lines intersect the origin and thus
are true lines of a constant percentage
restraint. The transition region between the
two breakpoints and slopes is approximated
by a third-order function (Fig. 2b).

The implemented characteristic allows
shaping the operate/restrain regions in
a flexible way. The following setting rules
apply:

\[ B_L \] lower breakpoint marks the AC-saturation-
free region; it is assumed that below this
value CT saturation will not occur due
to the AC component even with 80%
residual flux.

\[ B_H \] higher breakpoint marks the AC-saturation
region; it is assumed that above this value
CT saturation will occur due to the AC
component alone even with 0% residual
flux.

\[ S_L \] lower slope controls sensitivity of protection
under low currents; it should be set above
maximum spurious differential current
with no CT saturation.

\[ S_H \] higher slope recommended to be set at
about 60%; this value is of a secondary
importance, as stability of the algorithm
does not depend on the differential
characteristic alone.

CT saturation detection combines three
distinctive parts:

First, fast saturation due to large AC current
components is detected. Second, slower
saturation under small AC currents, but
significant and long-lasting DC currents is
detected. Third, extra security measures
applied after detecting CT saturation are kept
in place for an extended period of time by a
dedicated memory circuit. This is required
because the applied CT saturation detection
techniques are of a transient nature and will
not latch themselves.

Memory of the CT saturation detection
logic

The saturation flag, SAT, is set by a state-
machine shown in Fig. 3. Normally, the state
machine is operating in the “NORMAL” state.

A saturation condition, SC, described later
causes transition to the “EXTERNAL FAULT”
state. The saturation flag is set at this time.
Normally, no CT saturation occurs yet. In order
to reset the “EXTERNAL FAULT” state, a RESET-1
condition must be present for 100msec. The
RESET-1 condition requires the differential
current to be below the lower slope or below
the pickup of the characteristic with no
saturation condition asserted:

\[ \text{RESET-1} = (I_D < S_L \cdot I_R) \text{ OR } (I_D < P) \text{ AND NOT} \text{ (SC)} \quad (4) \]

While in the “EXTERNAL FAULT” state, the
state machine may step further into the
“EXTERNAL FAULT WITH CT SATURATION” state.
This is programmed to occur if the differential
characteristic is entered while in the “EXTERNAL
FAULT” state. In order to reset the “EXTERNAL

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Equation (6) declares CT saturation due to AC components if the restraining current is above the lower breakpoint (boundary of guaranteed saturation-free CT operation), while the differential current is relatively low (no differential pickup). Graphically, the AC saturation detection may be illustrated as a differential/restraining current trajectory flying through a particular window as depicted in Fig. 4a. Under subsequent CT saturation, condition (6) would reset, hence the need for the CT saturation memory circuit discussed above and shown in Fig. 3.

**DC saturation detection**

DC saturation occurs due to long-lasting DC components in the currents, even if both the AC and DC components are relatively low. Relative DC components are used in this algorithm as predictors of CT saturation. First, the DC components are calculated over one-cycle windows for both the neutral-side and terminal-side currents:

\[
I_{dc}(n) = \frac{I}{N} \sum_{k=0}^{N-1} (n-k)
\]

Where \( N = 64 \) s/c.

Second, presence of significant DC components in the terminal-side and neutral-side currents is checked using the AC components as adaptive thresholds:

\[
DC_c = I_{dcT} > D_1 \quad \text{AND} \quad |I_{N}| > P
\]

\[
DC_n = I_{dcN} > D_1 \quad \text{AND} \quad |I_{R}| > P
\]

Significant DC current is detected if the DC component is higher than a certain portion of the AC magnitude (D1) and the AC magnitude is greater than the pickup threshold of the differential characteristic. The latter condition is introduced to prevent detection of DC components on very low currents where small DC offset of the relay A/D converter may impact the algorithm. D1 is a factory constant of 0.25.

**Directional principle**

When CT saturation is detected, the stator differential function is not blocked or delayed, but extra security measures are applied. Effectively, the relay switches to a 2-out-of-2 logic with the differential and phase-comparison protection principles working in parallel. The phase comparison principle checks the relative direction of the neutral-side and terminal-side currents (Fig. 5a,b). Both the currents must be relatively high in order to check the direction. If at least one current is low, the angle is not checked and permission to trip is granted. In order to maintain high sensitivity and avoid user settings that may be difficult to calculate, the currents are compared in an adaptive way using the raw restraining current (2) as a base:

\[
\begin{align*}
\text{If} \ (|I_{R1}| > B_1 \ \text{OR} \ (|I_{N}| > D_1 \quad \text{AND} \quad |I_{R}| > P)) \ \text{AND} \\
\text{IF} \ (|I_{R2}| > B_1 \ \text{OR} \ (|I_{R1}| > D_2 \quad \text{AND} \quad |I_{N}| > P))
\end{align*}
\]

then \( \text{DIR}_c := \text{abs}(|\text{angle}(I_{R1})-\text{angle}(I_{N})|) > 90^\circ \) (11b)

else \( \text{DIR}_c := \text{true} \) (11c)

\( D_2 \) is a factory constant of 0.25.

The auxiliary directional flag created by equation (11) is conditioned with extra logic for solid performance during switch-off transients and other conditions (Fig. 5c).

**Adaptive logic**

The algorithm uses adaptive logic to combine the differential protection principle (DIF flag), saturation detection logic (SAT flag) and the phase-comparison protection principle (DIR flag). If no CT saturation is detected, the differential principle alone is capable of tripping the generator. If CT saturation is detected, both the differential and directional principles must pickup in order to trip. The operate flag (OP) is thus set as shown in Fig. 5d.
inrush. The fully offset current is at the level of 2.1 of CT nominal. The associated DC component was enough to saturate one of the CTs as soon as in 2 cycles (Fig. 7b) resulting in enough spurious differential current to cause misoperation of the installed relay. The new algorithm is stable for this case (OP flag).

Conclusions
A new algorithm for stator differential protection has been presented. The algorithm addresses extreme cases of CT saturation including both AC saturation under large currents and DC saturation under small but DC-offset currents. While ensuring good sensitivity and excellent security, the trip time of the actual relay hardware implementing the presented algorithm is below one power cycle. The described algorithm is a standard function on commercially available generator [2] and motor [3]numerical relays with more than one five hundred of unit-years of combined field experience to date.

References
Contact David Proctor-Golding, IST Energy, Tel (012) 426-7200, davidpg@ist.co.za

Numerous simulations and the up-to-date filed experience show that the adaptive logic of Fig. 5 ensures an excellent balance between speed, sensitivity and security. Nevertheless, the three critical flags (DIF, DIR and SAT) are available in user-programmable logic for custom applications.

Sample test results
Two field examples collected in North and South Americas as an outcome of misoperation of originally installed relays are presented. Results of waveform playback to the enhanced relay [2] are discussed below.

Example 1. Load change.
Fig. 6 presents a case of load change. The current is at the level of 0.3 of CT nominal, increasing to about 0.5 of nominal. The associated DC component was enough to saturate one of differential current to cause misoperation of the installed relay. The new algorithm detects CT saturation (SAT) well before the differential principle misoperates (PKP). The directional element restrains on this through-current condition (DIR), and the stator differential protection remains stable (OP).

Example 2. Transformer inrush. Fig. 7 presents a case of transformer magnetizing inrush. The fully offset current is at the level of 2.1 of CT nominal. The associated DC component was enough to saturate one of the CTs as soon as in 2 cycles (Fig. 7b) resulting in enough spurious differential current to cause misoperation of the installed relay. The new algorithm is stable for this case (OP flag).