Breakdown voltages of 65 V and higher allow LDMOS FETs to retain ruggedness and reliability while operating with 28 V power supplies. This article outlines the characteristics of such FET devices, and describes various methods of biasing to obtain best performance.

**LDMOS characteristics**

The laterally diffused metal-oxide-semiconductor (LDMOS) FET structure (Fig. 1) provides a 3-terminal device whose n+ source and drain regions are formed in a p-type semiconductor substrate. A laterally diffused, low-resistance p+ “sinker” connects the source region to the p+ substrate and source terminal. That configuration allows the substrate to be soldered directly to RF ground, thereby minimising the effect of wiring parasitics.

The gate region is isolated from the conducting channel by a thin layer of SiO₂. Applying a positive voltage to the gate with respect to the source allows current to flow between drain and source by forming an inversion layer (or channel) between the two n-type regions. LDMOS FETs operate in “enhancement mode,” meaning the drain-source current cannot flow until an applied positive gate voltage enhances a channel across the p-well.

When the FET is used as an amplifier, the channel current is modulated by an AC signal mixed with the positive gate-bias voltage. Fig. 2 shows the typical relationships between drain current and gate voltage at various temperatures. In contrast, note that RF devices such as GaAs FETs and MESFETs require a negative gate-bias voltage with respect to the source.

**Bias issues**

As the temperature of an LDMOS FET increases, its gate threshold shifts, its gₘ, and its Rₛ(on) goes down. These effects are usually shown in the data sheet as a plot in which the gate bias values are normalised to 1 V at 25°C, and different curves show the bias change needed to maintain given drain currents over temperature (Fig. 3). LDMOS FETs have a positive coefficient at low drain currents, but at more useful operating currents the coefficient becomes negative, giving protection against thermal runaway. The FET’s performance in a power amplifier is a tradeoff between linearity, efficiency, and gain, leading to an optimum drain-current setting that must be maintained over temperature, supply-voltage variation, bias-point shifts, and aging.

**Traditional bias methods**

Fig. 4 shows two analogue methods for controlling gate bias. The simpler circuit Fig. 4(a), using a divider and diode (whose forward voltage changes -2 mV/°C) to reduce the variation of quiescent current over temperature, is handicapped by the difficulty in matching the compensation to the LDMOS FET and diode.

Circuit Fig. 4(b) introduces a trimmed temperature sensor to eliminate the diode variation. The op amp provides gain that matches the slope of temperature to the LDMOS device, and a manual potentiometer or EEPROM sets the starting point or offset. Circuit Fig. 4(b) is better than circuit Fig. 4(a), but both assume that a simple linear compensation of gate voltage vs. temperature is sufficient for maintaining a constant drain voltage. That is not necessarily so, especially for power amplifier designs. More accurate compensation requires a nonlinear adjustment. Moreover, such compensation schemes do not allow for changes in drain voltage to improve efficiency. The best approach for compensation combines analogue and digital with mixed-signal techniques.

**New devices**

A number of bias-control devices for LDMOS FETs in RF power amplifiers have been developed. They provide temperature compensation for class A and class AB power-amplifier configurations, and also provide automatic power control, by setting the Vgs level to optimise the drain current vs. variations in RF power and drain voltage. New devices that provide continuous control include the following:

- High-side current-sense amplifier for sensing drain current
- ADC for digitising drain current (Iₘ₇) during calibration and over temperature
- DAC for setting the gate bias voltage
- Non-volatile look-up table (temperature vs. gate voltage)
- Integrated alarm functions with gate-voltage clamping.

The continuous-control approach offers advantages: it reduces manufacturing cost by allowing automatic set up of the PA to improve set point accuracy, reduces the margins required in device selection, allows nonlinear compensation, and allows dynamic biasing when the PA output power is reduced during quiet periods. The overall scheme is shown in Fig. 5.

The front-end device is a dual LDMOS high-side sense amplifier and gate-driver amplifier. The high-side sense amplifier monitors the LDMOS FET’s drain current over the range 20 mA to 5A, using an external sense resistor scaled for different current levels. The chip provides a gain setting of 2 or 10, with a typical input-referred offset voltage of 0 V or 3 mV. (The 3 mV option is for applications that require offset nulling.)
The sense-amplifier output is referred to ground, with a maximum output voltage of 5 V. The drive amplifier is current limited and provided with a logic-controlled fast clamp to zero. The clamp is independent of the serial interface, in case the system controller detects a fault. That arrangement allows “fast” protection of the LDMOS FET. The amplifier is configured for a gain of either 2 or 4, to accommodate various LDMOS gate-voltage requirements. Output transients are limited to ±100 mV during power up and power down.

With application of power the gate-driver amplifier starts in a shutdown state, so the outputs from the sense and drive amplifiers are tied to ground through resistor networks. The devices draw only about 100 µA of supply current in that state. Toggling the external /SHDN input from low to high turns the part ON, which allows a controlled start-up and protects the LDMOS devices.

The dual RF LDMOS bias controller is a dual IC containing comprehensive circuitry for setting and controlling the bias for a dual RF LDMOS power device. It contains the current sense and gate-drive functions of the gate-driver amplifier (discussed above). Gain for the current-sense function is augmented by a programmable-gain amplifier (PGA) featuring auto calibration that is transparent to the user, allowing accuracy to be guaranteed over time and temperature.

Two external, current driven, diode-connected transistors can be used to monitor the temperature of the power devices, and an internal diode monitors the local die temperature. These temperatures, along with the drain currents and two spare inputs (which can be used for measuring drain voltage, RF power, or monitoring any other PA parameters) are multiplexed into the 12-bit ADC. The available options let you read an individual channel or scan all channels under internal or external control, and store the results in an internal FIFO.

On the control side, an 8-bit coarse DAC and 10-bit fine DAC generate a positive bias voltage for the gate drivers. The gate-voltage buffer is current limited, and (as for the gate-driver amplifier) includes a logic-controlled fast clamp to zero, independent of the serial interface for LDMOS protection. The ADC data, DAC setting, and control registers are all accessed by the host processor via a serial SPI or I²C interface (according to the connection at the interface select pin).

The most common application is a Class AB LDMOS amplifier with open-loop control. The processor, using a customer-defined lookup table and algorithm, sets the DACs to implement a digital control loop for controlling the LDMOS gate bias voltage. This approach is implemented in three stages:

**Characterisation**

A sample of LDMOS parts are characterised over temperature to determine (as a calibration curve) a set of gate-voltage values (from the DAC) that maintains a constant drain current. One assumes that the curve is fairly consistent from part to part. A group of parts at a given drain current may exhibit shifts in offset, but no dramatic changes in slope. The values are stored in a non-volatile lookup table (LUT) in the users system. Additional LUTs can make adjustments for other purposes, such as reducing drain voltage with output power.

**Calibration**

During production, the PA’s quiescent drain current is measured at a calibration temperature (usually room temp), and the
DAC value is adjusted until drain current falls within the limits specified for that temperature. The DAC VGS value is stored as an initialisation point. For single-point temperature calibration, the initialised value of VGS is compared with the ideal VGS value at the corresponding temperature from the look-up table. The difference between actual and ideal VGS is then stored as an offset for the particular device, and added to every value in the temperature look-up table. For 2-point temperature calibration of an LDMOS device, you can calculate the slope (gain) coefficient for a particular device, and achieve a first-order correction for gain by multiplying every value in the look-up table by the slope coefficient.

**Operation**

Periodically, the temperature of the LDMOS device is measured and compared with the previous reading. If it has changed, the host processor reads the LUT, obtains characterisation data, and updates the DAC to correct the drain current. Using a host processor to correct for changing temperature and other factors allows scope for more sophisticated corrections. The effects of aging, for example, could be built into the host algorithm, in addition to offset and changes in the slope of the calibration curve.

Control if the gate voltage (for temperature compensation and automatic power control) and integration of non-volatile lookup tables with interpolation is shown in (Fig. 6). The addition of a non-volatile lookup table allows for “set and forget” bias settings, and allows the bias controllers to regulate bias conditions without need for an external microcontroller. This self-contained biasing scheme removes all digital signalling on the RF board, and allows close placement of the bias controller to the actual LDMOS devices without worrying about digital feed through in the RF spectrum. The two independent DAC channels implement the following function:

\[ V_{\text{GATE}} = V_{\text{SET}} + LUT_{\text{TEMP}}(\text{Temp}) + LUT_{\text{APC}}(\text{APC}) \]

where \( V_{\text{GATE}} \) is the actual amplified gate voltage, \( V_{\text{SET}} \) is the factory-set gate voltage at \( T_{\text{CAL}} \), \( LUT_{\text{TEMP}}(\text{Temp}) \) is the interpolated lookup value in the TEMP table for the sampled temperature, and \( LUT_{\text{APC}}(\text{APC}) \) is the interpolated lookup value in the automatic power control (APC) table for the APC parameter.

Users have extensive control over the configuration of the lookup tables. Up to four independent LUTs may be defined (one for each independent variable for the two channels), and users may vary the LUT size according to the resolution requirements of each variable. If the DAC output is a function of only one variable, you can define either two LUTs (one for each channel) or one unified LUT of greater resolution, common to both channels.

In addition, 32 bytes of dedicated user memory can be used for storing any board or PA identification, or calibration data. By configuring smaller LUTs, additional user memory can be made available. A diagram (Fig. 7) describes the type of algorithm and potential pointers to the look-up-tables. The temperature coefficients are stored in 64 memory locations. Step size, table offset, and interpolation (1:2, 1:4 or 1:8) can be selected, enabling gate-voltage settings for temperature changes down to 0.25°C.

The parameter is stored in 32, 64, 128 or 192 memory locations, depending on the nonvolatile-memory configuration. As before, step size, table offset, and interpolation (1:2,
1:4 or 1:8) are selectable to enable gate-voltage settings for 18 mV changes in a 28 V drain supply.

The implementation of newer efficiency-enhancement schemes such as automatic power control rely on the fact that PA output power varies with time, depending on the distances between the mobile users and a fixed base station. For better efficiency, the system adjusts the gate voltage (or drain current) via the APC loop as output power or drain voltage is reduced.

LDMOS devices are characterised to determine values for the LUTs. At the calibration temperature, the DAC value is determined and stored in the non-volatile \( V_{GATE} \) set register. During operation, the ADC monitors temperature and another APC parameter. If either changes, the MAX11008 keeps the LDMOS drain current close to the ideal by selecting, through interpolation of the LUT values, another DAC correction value. With a drain current of 1 A and a 75 mW sense resistor the error is typically < 0.9%. With a drain current of 250 mA and a 300 mW sense resistor, the error is typically < 1.75%. Some of these devices can also be used for monitor and control functions in PA-linearisation loops and other RF applications.

The MAX11010 and MAX11011 are equivalent to the MAX11008, but without the capabilities for drain current sensing and LDMOS gate drive. For greater design flexibility data converters are available which offer a multi-channel ADC with FIFO, on-chip channel-scan mode and internal data averaging, a number of DACs and GPIOs, and an internal, ±1°C-accurate temperature sensor. These ADCs and DACs have either 10-bit or 12-bit resolutions.

MAX11014-11015 ICs are variations of the MAX11008. Having a negative instead of a positive gate drive, they are designed for MESFET or GaAs FET applications. To protect those FETs in the event of a fault, the gate drive can be clamped to an externally set voltage.

Summary

The integrated circuits described above allow the designer of a base-station power amplifier to implement the LDMOS bias as a complete and compact integrated circuit, or, with a few external components, to introduce flexibility in the design. These parts can also be used in industrial and automotive control loops to implement current sensing and temperature compensation. To aid in evaluating the parts, Maxim offers evaluation kits with calibration and setup software running on a PC.

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Fig. 6: MAX11008 block diagram.

Fig. 7: MAX11008 algorithm.