The issues driving the need for increased sophistication are portability, power savings, features and weight. The products that are pushing the envelope of sophistication include, wireless communication, digital consumer and internet infrastructure products. Other contributors that make designs more complex are convergence of computer and telecommunications technologies, i.e. wireless networks, wireless access protocols (WAP), and handheld device markup language (HDML). Silicon complexity produces new challenges for packaging and system design. Engineers constantly wrestle with increased design complexity, speed and density, as well as the interrelated effects of digital, analogue and RF requirements packed into the same product. All of that leads to the importance of accurate constraint-driven processes. Fig. 1 shows the leading technological causes that drive future designs.

Packaging challenges
The packaging growth of different components types used in designs are changing with BGA/CSP and COB/DCA components increasingly used in new designs (Fig. 2). Increased usage of BGA packages present challenges that strain design systems with higher I/O counts, all driving requirements for advanced semiconductor devices. Array-based I/O configuration of 1.5, 1.27, 1.00, 0.8 mm and smaller BGAs are common today but they have their own problems that encompass manufacturer handling and solderability, repair and compatibility with existing assembly processes.

Advanced packaging options are increasing, with the use of plastic ball grid array (PBGA, Fig. 3), tape ball grid array (TBGA, Fig. 4) as the most common types of BGAs.

One newer packaging option that is being used is chip scale packages (CSP, Fig. 5). This device is smaller than traditional BGAs because it is only 20% larger than the bare die and can accommodate low to medium I/O count. CSP is predominately used for memory applications.

Another type of BGA combines two to four cavities to accommodate multiple dies and is sometimes referred to as ‘system-in-a-package’. In addition, direct chip attach (DCA, Fig. 6) is gaining more popularity for high performance applications.

Design packaging decisions
With all that components engineers are faced with, decisions must be made on package type and whether to design packages in-house or farm them out. With any decision, they want to perform a fast package feasibility study to make sure the criteria for package selection and design rules for connecting the die work. Once decisions are finalised the real challenges become apparent when there are no specific die models or libraries to choose from. During IC design stage, designers are trying to constantly shrink the size of the die. And because of constant changes in parallel design processes, fast package feasibility studies are an essential step to ensure success. Even relying on an outside source to design packages requires a fast package feasibility study because each day’s delay in knowing if the die changed or if the I/O configuration still works with the chosen package is detrimental to meeting the window of opportunity. Some EDA vendors have responded to the advanced packaging challenges by incorporating modules inside traditional PWB design software to deal with designing the package and employing this capability to design with chip on board (COB) or laminated multi chip modules (MCM-L).

This additional functionality allows designers to capture die and I/O information to create a library decal in a short amount of time.
Standard data support
- GDSII, ASCII
- Data preview and filtering

Parametric construction
- Facilitates early package exploration and feasibility

Package footprint
- Template-driven construction
- De-population, centre array
- JEDEC pin naming

After the die information is captured, engineers can decide to create a symbol for wire bonding or flip chip. The criteria for choosing an appropriate style include:

Wire bonding
- Most common die attachment method
- Well-known, cost-effective technology
- Upper limit 800 -1000 I/O, 50-70µm pitch
- Multiple row/tier bonding
- Die flag and multiple power rings
- Bond wire inductance

Flip chip
- Direct connection from die pad to package substrate
- High I/O capable 1600-2000
- Leading choice for high-performance devices
- Require additional wafer level processing
- Underfill, CTE mismatch
- May require wafer level redistribution routing

Wire bonding has its own rules that change based on the foundry equipment used.

Substrate bond pad size
- Pitch
- Wedge or ball bonding
- Rework consideration

Clearances
- Wire bond to wire bond
- Wire bond to substrate bond pad
- Substrate bond pad to substrate bond pad

Flip chip presents different challenges, but they do require less space on the board.
- Complex via fanouts
- Repetitive escape patterns
- Differential signalling
- Build-up or additive substrate construction

Once the die design capture is finished, they are placed on the board and designed using EDA software as either a single BGA package or MCM-L design.

Conclusion
Design software that lacks the ability to design for increased demand of advanced packaging and MCM-L requirements severely limit a design engineer’s ability to respond quickly to time pressures and accommodate changes that are the reality of every design project. The goal is to stop using workarounds that are not efficient and demand new functionality from EDA vendors.

Contact Roelof Pelser, ASIC Design Services, Tel (011) 315-8316, roelof.pelser@asic.co.za