Companies that recognise this fact are struggling to accomplish this task today with a combination of MS Excel, white board sketches, emails, and internal “glue-ware”. Often, cross-team meetings are held, but there is no central repository for all the information and ideas that are exchanged. After the meeting ends, design team members go back into their individual silos and try to correctly recall and incorporate all that was discussed into their layout tool. This cycle repeats itself over and over in typical product release and is prone cross-team misunderstandings and human error.

**Proposed solution**

One of the key missing links for cross-team collaboration in the electronic design community is a single, graphical, interconnect and I/O planning/optimisation environment. This would allow design teams to see, in a single tool, the complete interconnect path from on-chip I/O to flip-chip bump, to package pin, and finally to PCB-level pin, displayed as a flight line. This ability to visualise the complete interconnect path across the system is the basis for optimal interconnect planning and gives an early indication of the routing challenges on the PCB and package substrate. Early schedule planning and costing could be more accurately calculated for the package substrate and PCB layout.

A big advantage of this approach would be to foster cross-team communications and promote a cross-fabric optimization methodology. Traditional flows that drive signal assignment from the IC out to the package and then from the package to the PCB would be supported. However, the flexibility to drive the signal assignment from the PCB, back up through the package and on to the IC would likely be more useful, particularly when the IC was in the early stages of floor-planning.

Many design tools on the market today require the user to enter detailed library data before they can get into physical planning. A restriction like this would be unacceptable to any cross-platform design tool and greatly limit acceptance by all design groups. Most physical library data can be automatically generated by simple software algorithms based on parametric data that is entered by the user. This approach should be used to extend the tools capabilities as a rapid prototyping and feasibility study environment. Temporary physical abstracts could be created on-the-fly for the die, package or PCB symbol. A user interface would prompt the user for all of the parameters needed to generate the physical footprint. These parameters would include physical extents, pin size, pin numbering styles (including JEDEC standards), and pitch. Temporary symbols could be easily replaced with the actual device when made available or the temporary symbol could be promoted to “approved” status once the librarian had validated it.

To speed up performance and to simplify the footprint view presented to each designer, a physical device should optionally be handled as an abstract. For example, the abstract for the IC would just contain overall extents and pad (I/O cells and bumps) locations. Additionally, the tool would ideally support layout hierarchy, allowing users another way to choose how any given physical device is presented to them. For detailed editing, this environment would allow users to link their preferred EDA layout tool to each physical device or abstract. With a single button click the user would be able to directly launch their physical layout tool, specific to their design domain. After completing detailed changes in their domain, an abstract would be written and automatically updated in the planning environment.

In the early design stages, the complete interconnect path between IC, package and...
PCB may not be fully defined. For example, in a new design, the package pin-out would likely be unassigned other than some fixed power and ground nets. Therefore this tool would need to support the ability to generate connectivity on-the-fly while looking at routability of a given substrate and any constraints that the user has entered. For example, differential signal assignment to adjacent pins must be closely followed. The tool would therefore need to understand the basic layer stack-up of the package substrate and printed circuit board. To support this, the tool would need the ability to import technology data from the industry standard layout tools. This technology data typically contains line widths and spacing that would also be important to determine routability of the assignment.

It should also have its own basic stack-up editor where a user could quickly define the basic cross-section for their layout and specify the routing layers. This data would be directly read by the optimisation and assignment algorithms.

Once all connectivity from the IC to the PCB was defined the user could use an optimisation feature to start to make trade-offs between each physical instance. The signal optimisation would be based on routability or shortest path based the users preference and should support the ability to optimise the entire signal path across IC, package and PCB or to focus on a section of the interconnect path at a time. This optimisation algorithm is really the heart of the tool and once all of the data is available in the tool, it would likely be the most frequently used feature in the flow allowing layout specialists from each design domain the ability to quickly look at trade-offs between the IC, package, and PCB layouts.

In addition to untangling interconnect; rule based algorithms would be used to optimise the I/O placement based on PCB level requirements. In the case of an FPGA, a simple rule file to define pin equivalency would be required for correct I/O reassignment. However, for a typical ASIC, the tool would need to support the physical replacement of I/O buffers based on optimisation at the package and PCB. This would necessitate support for peripheral I/O placement, including multiple rows and staggering. It would also require support for advanced area array I/O placement. The ICs block level floorplan should not be ignored when this optimisation takes place and could be used to help drive the optimal I/O placement.

Signal names often change as they traverse from the IC to the package and finally onto the PCB. In addition, pin names used by the different design groups are often different between the physical layout tools being used by these unique design groups. Therefore, signal/pin mapping between design tools would need to be managed automatically by the tool.

During these early planning stages is also the best time to start to look at system level timing and potential signal integrity issues. Pre-route analysis could be performed by representing interconnect as estimated transmission lines, and simple lumped equivalent circuits. The results from any analysis run at this stage could be used to define constraints that would be used to drive the routing on the package substrate and PCB during final implementation. This is also the ideal time to start to plan and analyse the power distribution network (PDN) across the PCB, Package and onto the IC. Integration with an accurate power integrity (PI) tool could prove invaluable. Early analysis data could be used to drive the correct signal to power ratio for the flip-chip bump array mentioned above. It could also be used to make trade-offs between on-package and PCB level decoupling.

Since very few companies rely on a single EDA vendor solution for IC, package and PCB layout, it would be critical that this environment support industry standard formats for the IC, package and PCB symbols. The tool would be able to output standard industry formats such as Verilog, LEF/DEF and SPEF for IC design. A pin map in Excel format, AIF and electrical constraint file would be output for IC package design. Footprint and placement data as well as constraints could be output in the standard PCB formats. This tool would be used on a part time basis by design engineers with different areas of expertise, therefore, a focus on ease-of-use while developing this tool would be paramount. If designed correctly it could potentially be of use to nontechnical individuals in marketing and elsewhere for early planning and costing estimation.

Summary

The overall cost of getting a new IC out the door and into production is something many companies are taking a serious look at in today’s market. A few industry leading companies are starting to recognise that product cycles and costs can be driven down by integrating IC, package substrate and PCB layout teams early in the design planning stages. A design tool is needed to facilitate this cross-team collaboration.

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