Introduction to high-speed design

Today, high-speed design issues are becoming part of almost every design. Even those designs operating at lower frequencies often have high-speed issues due to fast device edge rates found in newer IC devices and technologies. Electrical engineers are now being asked to ensure there are no signal integrity issues along with their normal work load.

The old fashioned approaches of design (rules of thumb) are becoming less of an option for engineers. While for certain technologies this approach may still work, even when it does it normally creates extra cost for the company. This cost is often created by over-constraining the board, possibly requiring extra time during placement and routing, extra routing layers, more board space than necessary or actual signal integrity problems that often cause board respins. Sometimes these rules of thumb under-constrain the board, which causes long debugging sessions and often board respins. In turn, these respins cause schedule delays, budget increases, and added engineering work. Instead, electrical engineers need a well defined procedure with tools that are easy to use.

Historical design methodologies

The beginning of high-speed design was done through trial and error and manual calculations. The first software tools to solve high-speed PCB issues were post layout analysis tools. These tools extracted the board parameters from the layout system after it had been completed and began flagging problems quite late in the design cycle. Previous designs that have been created by many companies have proven that the earlier on in the design process that signal integrity problems are identified, the cheaper the cost of migration. This is due to the fact that the further on in the process one gets, the more changes required to correct the problem. For instance, a problem found after layout may require schematic changes, part changes, design section reroutes, and possibly the replacement of key sections. Electrical engineers should continually check signal integrity issues throughout the design cycle. Therefore, simulation tool companies need to create tools that can work throughout the design process. Today, many tools are utilised before a schematic capture is started and continue all the way through the design process until Gerbers are created.

Suggested design flow

Signal integrity should be considered from the very beginning of a design. Generally, pre-layout signal integrity tools are utilised during the design definition (schematic capture) stage. One of the first steps in the design process is determining what technologies are to be utilised. Once this is done, it is important to do some experimentation on the selected device technologies, especially if the technology is new to the designer. Experimentation should occur before the schematic design and continue throughout the process. During this early phase, electrical engineer experiments with different topologies including star configuration, daisy chains, and how many receivers can a particular technology drive, etc. This gives the engineer the necessary knowledge to create the schematic with the proper technologies. Before and during the schematic creation, many items, such as termination schemes, are generally experimented with to determine the optimal termination type and value. This type of experimentation allows for a much faster learning curve when using new technologies in a design.

After the initial exploration phase, an electrical engineer generally moves on to trying to determine constraints or design rules. The problem that arises is that the engineer generally knows what types of electrical (e.g. delay, line and termination impedance), not physical, characteristics (e.g. line lengths, line widths, stackups) are acceptable. The idea behind this step is to transform the electrical characteristics into physical constraints. This is done by switching or sweeping different physical constraints and then viewing how the electrical characteristics of the resulting waveform are affected. At this stage, electrical engineers sweep line lengths, termination values, impedance, line widths, trace separations, stack-ups, and more. These are compared against delays, overshoot, undershoot, ring back, intersymbol interference, eye openings, etc. The engineer can either compare the different graphs or create graphs showing the electrical value compared to each physical value and any effects due to the variation.

Once the relationships are understood, engineers look for the solution spaces - groups of physical

Fig 1: The PADS design solution (HyperLynx) - links to most PCB/CAD systems.
constraints areas where the electrical parameters are met. These different physical values make up the solution space.

Once the solution spaces are understood, the time has come to turn them into constraints or design rules. This process is going to differ slightly, based on the type of rules the layout system accepts. The basic idea is to set appropriate design rules without creating electrical problems. The less stringent the design rules, the easier it is for the PCB designer or autorouter to actually route the board. These constraints should include net constraints, bus constraints, topology constraints, pin pair constraints, component constraints, placement constraints, differential pair constraints, and more.

Once the constraints are discovered, it is important to properly pass them to the layout engineer. Today most companies pass the constraints in a Word document or Excel spreadsheet, which may be adequate for small designs but may not be the best way to deal with this information. The preferred method is to place the constraints directly in the schematic system and pass them forward into the layout system through the netlist. Some schematic systems can take some constraint information while others cannot. If it is not possible to put any constraints into the schematic, it is suggested to put the rules directly in the layout system after netlist importation. If the constraints are placed in the schematic capture system, they end up in any of the design reuse elements or new revisions that anyone can create from that design. Having all the constraints possible in the schematic and layout system allows a company to interactively route, batch route, or run design rule checks at any time.

The next step in the design process is for the layout engineer to create the board outline and do an initial placement of the board. Then an initial placement analysis should be done using signal integrity tools. More advanced signal integrity tools can extract the placement of the board into their database and a batch analysis can be run based on the IBIS models and Manhattan distances between pins. This is normally considered the “best case” since real traces are longer in most instances and may contain vias. Therefore, if the analysis shows that the “best case” does not work or barely passes, it means that the placement must be revised. Any traces that fail the batch analysis process, plus any critical traces, are run individually to view the waveforms, giving the user an idea of how bad the signal problem is. Some signal integrity tools give the user the ability to experiment with trace length and part placement. The user can also experiment with other factors, such as terminations, topologies, technologies, and more, thus producing new or further refined constraints which are added to the schematic and/or layout design rule or constraint section.

The next step in the high-speed process is to route to the constraints. This is done using either an interactive route environment, a batch analysis or both. Most layout designers route the critical traces first, using an interactive route environment. The interactive route environment allows a user to route while maintaining all the design rules placed in the system. Some interactive route environments allow for pushing traces, adding accordions, match length, differential pair routing, and a lot more. Critical traces may also need to be routed using manual routing. These traces need to be checked for adherence to different rules during verification (discussed later). Once the critical traces are routed, they are locked down, at which point an autorouter may be used. An effective system will feature an autorouter which recognises the constraints entered in the design database, along with the ability to set up a solid routing strategy. Setting up a good routing strategy can help a design route more effectively, with fewer disconnects, and in less time.

After the design is properly routed, it is time to run design verification. The main checks that are important are manufacturability (e.g. clearance), signal integrity (high-speed constraints), and connectivity checks. On the high-speed side, it is important to check length, differential pair, and impedance constraints, test point placement, and more. The layout designer should ensure all of the engineer’s criteria are met. If all the constraints were met, a final post-layout signal integrity analysis can be run on the design to ensure there are no unexpected problems. If some constraints were compromised, a more detailed analysis may be necessary to ensure no signal integrity problems exist.

The first step in post-layout analysis is to perform a batch design analysis. Signal integrity programs should have the ability to define the electrical constraints for all nets. The tool should then be able to run signal integrity analysis on the entire design against these constraints. The reason it is important to do a full board batch analysis is that an engineer can never be sure what nets will be problematic. Nets that fail or are marginal, should be more closely scrutinised.

The next step in post layout analysis is to simulate individual nets. Nets where constraints were not met or failed during batch analysis, as well as critical highspeed nets should all be simulated during this analysis. Each net should be simulated and the resulting waveforms should be analysed for signal integrity issues including crosstalk, ringing, overshoot, undershoot, threshold crossings, etc.

After the simulation of the nets is complete, users need to figure out how to fix any problems that were found. Simulation tools allow a user to experiment with some elements like termination. In traditional methods, designers return to the layout to make changes and then run through the full post-layout analysis again. This process is repeated until a solution is found for all nets. The problem is that when changes to the layout are made, they often affect many nets. In other words, solving one problem can create others. The other issue is that many times the user does not know how to fix the problem. This problem has been solved by some signal integrity simulation tools. The tools allow users to transfer the post-layout data into their pre-layout signal integrity tools. This brings all the characteristics into the schematic including routes, stack-up, vias, etc. Once in the signal integrity schematic environment, a user can change any aspect of the design to experiment with how to fix the signal integrity issue. After solving the issue, the user should pass off the information to the PCB layout person to rework the board. Once the rerouting of the items is done in layout, the post-layout steps should be repeated. This process should be repeated until there are no signal integrity issues.

If the design contains multiple PCBs, it is important to simulate nets that cross between these boards. There can often be problems created by PCB interaction or even caused by the connectors and cables. During pre-layout analysis, it is often possible to create topologies that contain drivers and/or receivers from different boards with the interconnects, connectors, and cables. This step can help identify constraints properly for the entire system. If one of the boards has been completed, it is recommended to do simulation of the existing board with different potential topologies of the new board’s connections. This means that users need a simulation tool that allows them to connect boards with signal integrity schematics. Once all boards are completely laid out, it is recommended that users simulate the designs that interconnect with each other. If one of the boards is coming from an outside party, it may be possible to obtain the PCB layout. If this is the case, ask the vendor for an EBD file of their board. An EBD file is a behavioural model of how the board will act. An EBD model is like an IBIS model for a board.

Conclusion

Signal integrity used to be performed by specialists. However, more recently, high-speed design has become mainstream, which has caused more and more people to try and effectively deal with high speed issues. Besides understanding high-speed methodology, it is important to have the right methodology and simulation tools, which can aid the engineer and designer throughout the entire design process. By dealing with signal integrity during the entire design, a designer can reduce development time and rework, ultimately eliminating re-spins. This leaves engineers with more confidence in their board during prototyping and production.

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